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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,602	03/30/2001	Joseph Jeddeloh	MIC-4	6053

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,602	JEDDELOH, JOSEPH	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 1, 2005 has been entered.

Claim Objections

2. Claims 2, 21, 23, 24, 26, 29, 30, 31, 40 are objected to because of the following informalities:

- As per claim 2, "said the final tally" should be "said final tally".
- As per claims 21, 23, 24, 26, 29, 30, 31, 40, "provides a memory module interface" should be "provides said memory module interface".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 12, 41, 42 and 53 are rejected under 35 U.S.C. 102(a) as being anticipated by Olarig et al., US Patent 6134638, hereinafter Olarig.

5. In re claims 12 and 53, Olarig discloses a method and means thereof for selecting an operating speed of a memory module [114] interface in a computer system [100], said system comprising a central processing unit [102], a memory controller [200], and at least one memory module comprising a serial presence detect memory [col.3, l.64 – col.4, l.37; col.4, l.56 – col.5, l.5; col.9, ll.51-64], said method and means thereof comprising:

- Generating multiple clock signals [memory clocks] at different frequencies to provide selectable operating speeds of said memory module interface [col.4, l.56 – col.5, l.5].
- Obtaining information from said serial presence detect memory that includes at least a speed grade [preferred clock frequency] of said memory module [col.10, ll.26-37].
- Selecting one of said operating speeds of said memory module interface in accordance with said obtaining information [col.9, ll.39-66].

6. In re claim 41, Olarig discloses a memory controller [200] comprising a memory module interface [fig.2] to at least one memory module [114], said memory module including serial presence detect memory [col.9, ll.51-64], wherein said memory controller [col.3, l.64 – col.4, l.37; col.4, l.56 – col.5, l.5]:

- Accesses serial presence detect memory [col.10, ll.26-47].
- Generates multiple clock signals [memory clocks] at different frequencies [col.4, l.56 – col.5, l.5].
- Obtains information from said serial presence detect memory [col.10, ll.26-37].
- Selects one of said clock signals for driving said memory module interface based on said obtained information [col.9, ll.39-66].

7. As to claim 42, Olarig discloses, wherein said obtained information comprises a speed grade [preferred clock frequency] of said memory module [col.10, ll.26-37].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 5-7, 9-10, 43-45, 47-49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig, in view of Ikeda, US Patent 6487086, and Schwartz, US Patent 4468729.

10. In re claims 1 and 43, Olarig discloses a method and means thereof for selecting an operating speed of a memory module [114] interface in a computer system [100], said system comprising a central processing unit [102], a memory controller [200], and at least one memory module comprising a serial presence detect memory [col.3, l.64 – col.4, l.37; col.4, l.56 – col.5, l.5; col.9, ll.51-64], said method and means thereof comprising:

- Generating multiple clock signals [memory clocks] at different frequencies to provide selectable operating speeds of said memory module interface [col.4, l.56 – col.5, l.5].
- Selecting one of said operating speeds of said memory module interface [col.3, ll.6-16].

11. Olarig did not disclose explicitly the counting of the number of the memory modules and did not disclose selecting the operating speed of the memory module interface based on the number of the memory modules.

12. Ikeda discloses a method and means thereof for selecting an operating speed of a memory module [10c] interface in a computer system [personal computer], said system comprising a central processing unit [inherent to process data], a memory controller [inherent to access data], [col.1, ll.11-35] said method and means thereof comprising:

- Generating multiple clock signals at different frequencies [100-133 MHz] to provide selectable operating speeds of said memory module interface [col.1, ll.45-62].
- Selecting one of said operating speeds of said memory module interface based on at least a final tally of the number of said memory modules [col.1, ll.45-62; operating speed and number of memory modules are matched to avoid reflections and distortions of signals].

13. It would have been obvious to one of ordinary skill in the art, having the teachings of Olarig and Ikeda before him at the time the invention was made, to modify the system taught by Olarig to include the teachings of Ikeda, in order to avoid reflections and distortions of signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to account for limitations in signal transmissions caused by reflections and distortions in conventional memory structures [Ikeda: col.1, ll.32-35, ll.60-62].

14. Schwartz discloses a method and means thereof comprising counting the number of memory modules and keeping a running tally [count] of the number of said memory modules based on said counting [col.5, ll.25-42].

15. It would have been obvious to one of ordinary skill in the art, having the teachings of Olarig and Schwartz before him at the time the invention was made, to modify the system taught by Olarig to include the teachings of Schwartz, in order to determine available memory capacity. One of ordinary skill in the art would have been motivated to make such a combination as it

provides a way ensure sufficient memory capacity for proper operation [Schwartz: col.2, ll.33-36].

16. As to claims 2 and 44, Ikeda discloses, wherein said selecting comprises generating memory module interface signals comprising clock, address, and data signals at a frequency based on said final tally of the number of said memory modules [col.1, ll.45-62; synchronize command operations and data transfers].

17. As to claims 3 and 45, Olarig discloses, comprising obtaining information from said serial presence detect memory that includes at least one characteristic [information] of said memory module, wherein said selecting comprises selecting one of said operating speeds in accordance with one of said final tally of the number of said memory modules and said characteristic [col.9, ll.39-66].

18. As to claims 5 and 47, Olarig discloses, wherein said characteristic comprises a speed grade [preferred clock frequency] of said memory module [col.10, ll.26-37].

19. As to claims 6 and 48, Olarig discloses, wherein said characteristic comprises a manufacturer of said memory module [col.10, ll.1-37].

20. As to claims 7 and 49, Olarig discloses, wherein said characteristic comprises a type of said memory module [col.9, ll.39-50].

21. In re claim 9, Olarig, Ikeda and Schwartz disclose each and every limitation of the claim as discussed above in reference to claims 1 and 3.

22. As to claim 10, Olarig, Ikeda and Schwartz disclose each and every limitation of the claim as discussed above in reference to claims 7 and 9.

23. In re claims 51, Olarig, Ikeda and Schwartz disclose the method as discussed above in reference to claim 9. Therefore, Olarig, Ikeda and Schwartz disclose the apparatus to which the method is operated on.

24. Claims 4, 8, 11, 46, 50 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig, Ikeda and Schwartz as applied to claims 3, 45 and 51 above, and further in view of Johnson et al., US Patent 5577236, hereinafter Johnson, in view of Chang et al., US Patent 5610543, hereinafter Chang.

25. Olarig, Ikeda and Schwartz disclose each and every limitation as discussed above in reference to claims 3, 45 and 51. Olarig, Ikeda and Schwartz did not disclose explicitly the characteristic comprising the number of components in each memory module and a physical layout of signal connections between the memory controller and the memory module.

26. Johnson discloses a method comprising obtaining information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors] of a memory module, wherein a selecting comprises selecting one of the clocks [Chang: col.31, ll.5-8; one of ordinary skill in the art would have selected a lower frequency instead of delaying the clocks to increase the data valid window in order to reduce power consumption] in accordance with one of said final tally of the number of said modules and said characteristic [col.8, ll.33-45; col.9, ll.4-18].

27. In re claims 4, 11, 46 and 52, Johnson discloses said characteristic comprises the number of components [memory circuits] in each said memory module [col.9, ll.9-10].

28. In re claims 8 and 50, Johnson discloses said characteristic comprises a physical layout of signal connections between said memory controller and said memory module [col.9, ll.11-16].

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Chang, Olarig, Ikeda and Schwartz before him at the time the invention was made, to modify the system taught by Olarig, Ikeda and Schwartz to include teachings of Johnson and Chang, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data with reduced power consumption [Chang: col.31, ll.5-8] from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

30. Claims 13-15, 17-19, 25-27, 30-32, 34-36, 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig in view of Stevens et al., US Patent 6226729, hereinafter Stevens, in view of Ikeda.

31. In re claim 13, Olarig discloses a computer system [100] comprising:

- A central processing unit [102].
- A memory controller [200] including a memory module interface [fig.2].
- At least one memory module [114] including a serial present detect memory [col.9, ll.51-64].
- Wherein said memory controller:
    - Generates multiple clock frequencies [503, 505, 507, 509] [fig.6; col.4, l.56 – col.5, l.5; col.11, l.39 – col.12, l.38].
    - Accesses said serial presence detect memory [col.9, ll.51-64].

32. Olarig did not disclose explicitly the keeping a running tally of the number of the memory modules based on the accesses to the serial presence detect memory and did not disclose

selecting the operating speed of the memory module interface based on the number of the memory modules.

33. Stevens discloses a computer system [fig.5] comprising:

- A central processing unit [595].
- A memory controller [500] including a memory module interface [530, 540, 544].
- At least one memory module [RIMM 570] including a serial presence detect memory [572].
- Wherein said memory controller:
    - Generates multiple clock frequencies [col.13, ll.41-49; Applicant's admission on page 3 of Remarks dated November 16, 2004].
    - Accesses said serial presence detect memory [col.11, l.66 – col.12, l.14].
    - Keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory [fig.8a, 850; col.12, ll.62-67; table 4].
    - Selects one of the clock frequencies [channel frequency] for driving said memory module interface based on at least a final tally of the number of said memory modules [col.13, ll.41-45; frequency selected based on final tally number of memory modules that are operable with frequency].

34. Stevens did not disclose explicitly a motivation for selecting one of the clock frequencies for driving said memory module interface based on at least a final tally of the number of said memory modules.

35. Ikeda discloses a method of selecting an operating speed of a memory module [10c] interface in a computer system [personal computer], said system comprising a central processing unit [inherent to process data], a memory controller [inherent to access data], [col.1, ll.11-35] said method comprising:

- Generating multiple clock signals at different frequencies [100-133 MHz] to provide selectable operating speeds of said memory module interface [col.1, ll.45-62].
- Selecting one of said operating speeds of said memory module interface based on at least a final tally of the number of said memory modules [col.1, ll.45-62; operating speed and number of memory modules are matched to avoid reflections and distortions of signals].

36. It would have been obvious to one of ordinary skill in the art, having the teachings of Olarig, Stevens and Ikeda before him at the time the invention was made, to modify the system taught by Olarig to include the teachings of Stevens, in order to avoid reflections and distortions of signals [Ikeda: col.1, ll.32-35, ll.60-62]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to account for limitations in signal transmissions caused by reflections and distortions in conventional memory structures.

37. As to claim 14, Olarig discloses, wherein said central processing unit is a microprocessor [col.4, ll.12-19].

38. As to claim 15, Olarig discloses, wherein said memory controller obtains information from said serial presence detect memory that includes at least one characteristic [information] of each said memory module [col.9, ll.39-66].

39. As to claim 17, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 5 and 15.

40. As to claim 18, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 6 and 15.

41. As to claim 19, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 7 and 15.

42. In re claim 25, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claim 13.

43. In re claim 26, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 13 and 15.

44. As to claim 27, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 19 and 26.

45. In re claim 30, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 17 and 26.

46. In re claim 31, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claim 13.

47. As to claim 32, Olarig discloses, wherein said memory controller obtains information from said serial presence detect memory that includes at least one characteristic [information] of said memory module, wherein said clock rate is also based on said characteristic [col.9, l.39 – col.10, l.37; preferred clock frequency according to characteristic must be considered with limitation imposed by Ikeda as discussed above].

48. As to claim 34, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 17 and 32.

49. As to claim 35, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 18 and 32.

50. As to claim 36, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 19 and 32.

51. In re claim 38, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 13 and 15.

52. In re claim 39, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 17 and 38.

53. Claims 16, 20, 28-29, 33, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig, Stevens and Ikeda as applied to claims 15, 26, 32 above, and further in view of Johnson, in view of Chang.

54. Olarig, Stevens and Ikeda disclose each and every limitation as discussed above in reference to claim 15, 26, 32. Olarig, Stevens and Ikeda did not disclose explicitly the characteristic comprising the number of components in each memory module and a physical layout of signal connections between the memory controller and the memory module.

55. Johnson discloses a method comprising obtaining information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors] of a memory module, wherein a selecting comprises selecting one of the clocks [Chang: col.31, ll.5-8; one of ordinary skill in the art would have selected a lower frequency instead of delaying the clocks to increase the data valid window in order to reduce power consumption] in accordance with one of said final tally of the number of said modules and said characteristic [col.8, ll.33-45; col.9, ll.4-18].

56. In re claims 16, 29, 32, Johnson discloses said characteristic comprises the number of components [memory circuits] in each said memory module [col.9, ll.9-10].

57. In re claims 20, 28, 37, Johnson discloses said characteristic comprises a physical layout of signal connections between said memory controller and said memory module [col.9, ll.11-16].

58. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Chang, Olarig, Stevens and Ikeda before him at the time the invention was made, to modify the system taught by Olarig, Stevens and Ikeda to include teachings of Johnson and Chang, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data with reduced power consumption [Chang: col.31, ll.5-8] from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

59. Claims 21, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig, Stevens and Ikeda as applied to claims 13, 15, 17 and 31 above, and further in view of Hartwell, U.S. Patent 6724850.

60. In re claim 21, Olarig, Stevens and Ikeda disclose each and every limitation as discussed above in reference to claims 13 and 15.

61. In re claim 24, Olarig, Stevens and Ikeda disclose each and every limitation as discussed above in reference to claims 13, 15 and 17.

62. Olarig, Stevens and Ikeda did not discuss the details of generating different frequencies.

63. Hartwell discloses a computer system [data processing system 100] comprising:

- At least two phase locked loops [PLL 1 and 3] to generate respective clock signals of different frequencies [slow and fast] [col.2, l.52 – col.3, l.10].

64. It would have been obvious to one of ordinary skill in the art, having the teachings of Hartwell, Olarig, Stevens and Ikeda before him at the time the invention was made, to use the phase locked loops taught by Hartwell for the system disclosed by Olarig, Stevens and Ikeda as the phase locked loop taught by Hartwell is a well known circuit suitable for generating different frequencies for the system of Olarig, Stevens and Ikeda. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to generate different frequencies in a system that require different clock speeds [Hartwell: col.1, l.56 – col.2, l.49].

65. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartwell, Olarig, Stevens and Ikeda as applied to claims 21 above, and further in view of Johnson, in view of Chang.

66. Hartwell, Olarig, Stevens and Ikeda disclose each and every limitation of the claim as discussed above in reference to claims 21. Hartwell, Olarig, Stevens and Ikeda did not disclose explicitly the characteristic comprising the number of components in each memory module.

67. Johnson discloses a method comprising obtaining information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors] of a memory module, wherein a selecting comprises selecting one of the clocks [Chang: col.31, ll.5-8; one of ordinary skill in the art would have selected a lower frequency instead of delaying the clocks to increase the data valid window in order to reduce power consumption] in accordance with one of said final tally of the number of said modules and said characteristic, wherein said characteristic comprises the number of components [memory circuits] in each said memory module [col.8, ll.33-45; col.9, ll.4-18].

68. It would have been obvious to one of ordinary skill in the art, having the teachings of Chang, Johnson, Hartwell, Olarig, Stevens and Ikeda before him at the time the invention was made, to modify the system taught by Hartwell, Olarig, Stevens and Ikeda to include teachings of Johnson and Chang, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data with reduced power consumption [Chang: col.31, ll.5-8] from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

69. Claim 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig as applied to claim 41 above, and further in view of Hartwell and Johnson in view of Chang.

70. Olarig discloses each and every limitation as discussed above in reference to claim 41. Olarig did not discuss the details of generating different frequencies and did not disclose explicitly the characteristic comprising the number of components in each memory module.

71. Hartwell discloses a computer system [data processing system 100] comprising:

- At least two phase locked loops [PLL 1 and 3] to generate respective clock signals of different frequencies [slow and fast] [col.2, l.52 – col.3, l.10].

72. It would have been obvious to one of ordinary skill in the art, having the teachings of Olarig and Hartwell before him at the time the invention was made, to use the phase locked loops taught by Hartwell for the memory controller disclosed by Olarig as the phase locked loop taught by Hartwell is a well known circuit suitable for generating different frequencies for the system of Olarig. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to generate different frequencies in a system that require different clock speeds [Hartwell: col.1, l.56 – col.2, l.49].

73. Johnson discloses a method comprising obtaining information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors] of a memory module, wherein a selecting comprises selecting one of the clocks [Chang: col.31, ll.5-8; one of ordinary skill in the art would have selected a lower frequency instead of delaying the clocks to increase the data valid window in order to reduce power consumption] in accordance with one of said final tally of the number of said modules and said characteristic, wherein said characteristic comprises the number of components [memory circuits] in each said memory module [col.8, ll.33-45; col.9, ll.4-18].

74. It would have been obvious to one of ordinary skill in the art, having the teachings of Chang, Johnson and Olarig before him at the time the invention was made, to modify the system taught by Olarig to include teachings of Johnson and Chang, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data with reduced power consumption [Chang: col.31, ll.5-8] from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

Response to Arguments

75. Applicant's arguments filed on June 1, 2005 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Tse Chen
July 30, 2005